REMARKS

In the Office Action dated March 17, 2005, the Examiner rejected claim 1 under 35 USC 112, second paragraph, as being indefinite, rejected claims 1-7 and 9-11 under 35 USC 102 as anticipated by Lin (US Patent No. 6,483,147) and rejected claims 8 and 15-16 under 35 USC 103 as unpatentable over Lin and Mitani (US Publication 2003/0057491). The Applicants acknowledge that claims 17-25 have been withdrawn. Claims 1-16 remain at issue.

The 35 USC 112, Second Paragraph Rejection

The Applicants are confused by the Examiner's 35 USC 112, second paragraph rejection. In the Office Action, the Examiner states the limitation "active silicon layer" in claim 1 lacks an antecedent basis. A review of claim 1 as filed, however, shows the word "an" before the limitation. The proper antecedent basis therefore appears to be present. The Applicants assume that the Examiner simply overlooked the proper antecedent basis. If not, the Applicants would like a more detailed explanation of the rejection.

The Art Rejection

The Examiner has indicated that some of the claims of the present application are anticipated by Lin. The Applicants strongly disagree. Lin does not anticipate any of the claims of the present application.

The Lin reference specifically teaches that a MOSFET 42 is formed on top of the device layer 32. See Figure 7 and column 6, lines 47-54. The Lin reference therefore does not teach or suggest a transistor formed in the active silicon layer as recited in the claims of the present invention. The claims of the present invention are therefore not anticipated by Lin.

Furthermore, it would not be proper to combine the Lin and Mitani references to find any of the claims of the present application as obvious. Since the heat generating MOSFET 42 is formed on top of the device layer 32 of Lin, there would

be little if any reason to modify the Lin reference to use the isolation films 4 of Mitani to electrically isolate adjacent transistors formed in the semiconductor layer 3a, as shown in Figure 3 of Mitani. In other words, since the MOSFETS 42 of Lin are formed above as opposed to within the device layer 32, there is no apparent reason to form isolation regions in the device layer 32.

Lastly, the Applicants would like to point out that the Lin fails to teach or suggest using a thermally conductive paste such as a DAG in the plug formed in the bulk silicon layer. On the contrary, Lin teaches the use of a number of metals, alloys, nitrides and suicides thereof. Specifically, see column 3, lines 64-67 through column 4, lines 1-11 of Lin. Any claims reciting the use of a DAG are therefore not anticipated or obvious in view of the Lin or Mitani references, either separately or in combination.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

James W. Rose
Reg. No. 34,239

P.O. Box 70250
Oakland, CA 94612-0250
(650) 961-8300